3/6

February 21, 2003

File 344:Chinese Patents Abs Aug 1985-2003/Jan
(c) 2003 European Patent Office
File 347:JAPIO Oct 1976-2002/Oct(Updated 030204)
(c) 2003 JPO & JAPIO
File 350:Derwent WPIX 1963-2003/UD,UM &UP=200312
(c) 2003 Thomson Derwent

Set	Items	Description
S1	69	AU='HEIN J' OR AU='HEIN J P'
S2	40	AU='SOOCH N' OR AU='SOOCH N S'
S3	11	S1 AND S2

3/5/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015028774 **Image available**
WPI Acc No: 2003-089291/200308
Related WPI Acc No: 1998-584026; 2000-116869; 2000-671729; 2000-686101; 2001-015037; 2001-181441; 2001-190654; 2001-234102; 2001-281144; 2001-431571; 2001-440036; 2002-009481; 2002-082016; 2002-120969; 2002-235397; 2002-236851; 2002-303142; 2002-749276; 2003-027952
XRPX Acc No: N03-070339

Telephone line termination circuit system that utilizes ring detection circuitry on both sides of isolation barrier hence provides significant reduction in power usage

Patent Assignee: SILICON LAB INC (SILI-N)
Inventor: **HEIN J P** ; SCOTT J W; **SOOCH N S** ; WELLAND D R
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6456712	B1	20020924	US 97837702	A	19970422	200308	B
			US 97837714	A	19970422		
			US 97841409	A	19970422		
			US 9834453	A	19980304		

Priority Applications (No Type Date): US 9834453 A 19980304; US 97837702 A 19970422; US 97837714 A 19970422; US 97841409 A 19970422
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6456712	B1		37	H04M-001/00	CIP of application US 97837702
					CIP of application US 97837714
					CIP of application US 97841409

Abstract (Basic): US 6456712 B1

NOVELTY - The ring detection circuits include ring burst circuits on the phone line side of the isolation barrier and ringer timing circuits on the powered side of the barrier. The digital burst peak signal is transmitted through the isolation barrier to the ringer timing circuits.

USE - As telephone line termination circuit.

ADVANTAGE - Provides significant reduction in the power usage on the telephone line side of the barrier.

DESCRIPTION OF DRAWING(S) - The drawing shows a block diagram of the system.

pp; 37 DwgNo 17/21

Title Terms: TELEPHONE; LINE; TERMINATE; CIRCUIT; SYSTEM; UTILISE; RING; DETECT; CIRCUIT; SIDE; ISOLATE; BARRIER; SIGNIFICANT; REDUCE; POWER
Derwent Class: W01; W02
International Patent Class (Main): H04M-001/00
International Patent Class (Additional): H04B-001/38; H04B-003/00; H04M-003/00
File Segment: EPI

3/5/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014928567 **Image available**
WPI Acc No: 2002-749276/200281
Related WPI Acc No: 1998-584026; 2000-116869; 2000-671729; 2000-686101; 2001-015037; 2001-181441; 2001-190654; 2001-234102; 2001-281144; 2001-431571; 2001-440036; 2002-009481; 2002-082016; 2002-120969; 2002-235397; 2002-236851; 2002-303142; 2003-027952; 2003-089291
XRPX Acc No: N02-589990

Digital isolation system used in telephone, modem, has bias voltage

generator connected to VCO during low-power operation so as to provide VCO output

Patent Assignee: SILICON LAB INC (SILI-N)
Inventor: DUPUIS T J; **HEIN J P** ; SCOTT J W; **SOOCH N S** ; TUTTLE G T; WELLAND D R
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6442271	B1	20020827	US 97837702	A	19970422	200281 B
			US 97837714	A	19970422	
			US 97841409	A	19970422	
			US 9834621	A	19980304	

Priority Applications (No Type Date): US 9834621 A 19980304; US 97837702 A 19970422; US 97837714 A 19970422; US 97841409 A 19970422
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6442271	B1		32	H04M-001/00	CIP of application US 97837702
					CIP of application US 97837714
					CIP of application US 97841409

Abstract (Basic): US 6442271 B1

NOVELTY - A phase locked loop (PLL) circuit is connected to an input of a voltage controlled oscillator (VCO) (336) during normal operation. A bias voltage generator is connected to the VCO input and the PLL circuit is disconnected from the VCO input during low-power operation so that the VCO output is provided even during low-power operation.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

(1) Telephone;
(2) Modem; and
(3) Isolation system operating method.

USE - For isolating electrical circuits used in telephone (claimed) such as cordless phones, speaker phone, etc., data communication device such as modem (claimed), also in industrial and medical applications.

ADVANTAGE - By connecting the bias voltage generator to VCO input during low-power mode operation, the isolation system is allowed to operate continuously even if the powered circuits are shut down, hence prevents dangerous or destructive voltage to enter into the isolation system and saves power, thereby improving communication reliability and reducing amplitude and phase noise interference.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the digital isolation system.

Voltage controlled oscillator (336)

pp; 32 DwgNo 17/17

Title Terms: DIGITAL; ISOLATE; SYSTEM; TELEPHONE; MODEM; BIAS; VOLTAGE; GENERATOR; CONNECT; VCO; LOW; POWER; OPERATE; SO; VCO; OUTPUT
Derwent Class: U23; W01
International Patent Class (Main): H04M-001/00
International Patent Class (Additional): H04M-009/00
File Segment: EPI

3/5/3 (Item 3 from file: 350)

DIALOG(R)File 350:Derwent WPIX

014300265 **Image available**
WPI Acc No: 2002-120969/200216
Related WPI Acc No: 1998-584026; 2000-116869; 2000-671729; 2000-686101; 2001-015037; 2001-181441; 2001-190654; 2001-234102; 2001-281144; 2001-431571; 2001-440036; 2002-009481; 2002-082016; 2002-235397; 2002-236851; 2002-303142; 2002-749276; 2003-027952; 2003-089291
XRPX Acc No: N02-090716

Telephone line isolation system output inhibition method for data

communication, involves restoring synchronization and framing lock in isolated circuit to end freeze mode operation after disruptive event occurs

Patent Assignee: SILICON LAB INC (SILI-N)
Inventor: DUPUIS T J; **HEIN J P** ; SCOTT J W; **SOOCH N S** ; TUTTLE G T; WELLAND D R
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6307891	B1	20011023	US 97837702	A	19970422	200216 B
			US 97837714	A	19970422	
			US 97841409	A	19970422	
			US 9834684	A	19980304	

Priority Applications (No Type Date): US 9834684 A 19980304; US 97837702 A 19970422; US 97837714 A 19970422; US 97841409 A 19970422
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6307891	B1		30	H04B-015/00	CIP of application US 97837702
					CIP of application US 97837714
					CIP of application US 97841409
					CIP of patent US 5870046
					CIP of patent US 6137827

Abstract (Basic): US 6307891 B1

NOVELTY - A disruptive event is identified in a master circuit (225) to send a freeze control signal to an isolated circuit (226). During freeze mode operation, output of the isolated circuit to outside of a telephone line isolation system (330) is inhibited. A synchronization and framing lock is restored in the isolated circuit after the disruptive event occurs to end freeze mode operation.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for telephone line isolation system.

USE - For telephony and data communication applications.

ADVANTAGE - As isolated circuit is placed in frozen state, errors occurring due to transfer of erroneous data and control signals, is prevented.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the telephone line isolation system.

Master circuit (225)

Isolated circuit (226)

pp; 30 DwgNo 17/17

Title Terms: TELEPHONE; LINE; ISOLATE; SYSTEM; OUTPUT; INHIBIT; METHOD; DATA; COMMUNICATE; RESTORATION; SYNCHRONISATION; FRAME; LOCK; ISOLATE; CIRCUIT; END; FREEZE; MODE; OPERATE; AFTER; DISRUPT; EVENT; OCCUR
Derwent Class: W01; W02
International Patent Class (Main): H04B-015/00
File Segment: EPI

3/5/4 (Item 4 from file: 350)

DIALOG(R)File 350:Derwent WPIX

014188784 **Image available**
WPI Acc No: 2002-009481/200201
Related WPI Acc No: 1998-584026; 2000-116869; 2000-671729; 2000-686101; 2001-015037; 2001-181441; 2001-190654; 2001-234102; 2001-281144; 2001-431571; 2001-440036; 2002-082016; 2002-120969; 2002-235397; 2002-236851; 2002-303142; 2002-749276; 2003-027952; 2003-089291
XRPX Acc No: N02-007874

Telephone communication system transmits signals across isolation barrier to provide power supply for portion of phone line integrated circuit

Patent Assignee: SILICON LAB INC (SILI-N)
Inventor: **HEIN J P** ; SCOTT J W; **SOOCH N S** ; WELLAND D R

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6298133	B1	20011002	US 97837702	A	19970422	200201	B
			US 97837714	A	19970422		
			US 97841409	A	19970422		
			US 9834802	A	19980304		

Priority Applications (No Type Date): US 9834802 A 19980304; US 97837702 A 19970422; US 97837714 A 19970422; US 97841409 A 19970422
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6298133	B1		41	H04M-001/738	CIP of application US 97837702
					CIP of application US 97837714
					CIP of application US 97841409
					CIP of patent US 5870046
					CIP of patent US 6137827

Abstract (Basic): US 6298133 B1
NOVELTY - A phone line side integrated circuit (118) is coupled to powered side circuitry (116) through an isolation barrier (110). Signals transmitted across the isolation barrier, provides power supply for a portion of the phone line integrated circuit within which a ring detection and caller ID circuitry (1704) with their respective inputs are integrated.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(a) Interface architecture;
(b) Communication system provision method;
(c) Caller ID and ringer data providing method
USE - Telephone communication system provided with isolation systems for selectively isolating electrical circuit from one another, used in telephony, medical, electronics and industrial process control applications.
ADVANTAGE - Line side convertors are powered from phone line while using standard hook-switch and diodes without need for expensive low voltage drop hook-switch and diodes. By using common inputs for the ringer circuitry and the caller ID circuitry, the need for a separate caller ID interface is eliminated. Since the voltage levels on the lines are within standard integrated circuit technology limitations, the requirement for separate high voltage switches for inputting caller ID data is eliminated, thus the cost and system board space usage is lowered.
DESCRIPTION OF DRAWING(S) - The figure shows the communication system.
Isolation barrier (110)
Powered side circuitry (116)
Phone line side integrated circuit (180)
Ring detection and caller ID circuitry (1704)
pp; 41 DwgNo 17/21
Title Terms: TELEPHONE; COMMUNICATE; SYSTEM; TRANSMIT; SIGNAL; ISOLATE; BARRIER; POWER; SUPPLY; PORTION; TELEPHONE; LINE; INTEGRATE; CIRCUIT
Derwent Class: W01
International Patent Class (Main): H04M-001/738
International Patent Class (Additional): H04M-019/00
File Segment: EPI

3/5/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013955822 **Image available**
WPI Acc No: 2001-440036/200147
Related WPI Acc No: 1998-584026; 2000-116869; 2000-671729; 2000-686101;

2001-015037; 2001-181441; 2001-190654; 2001-234102; 2001-281144; 2001-431571; 2002-009481; 2002-082016; 2002-120969; 2002-235397; 2002-236851; 2002-303142; 2002-749276; 2003-027952; 2003-089291
XRPX Acc No: N01-325387

Communication system used in telephony, has capacitive interface that couples hookswitch, caller ID and ringer interface circuit to phone lines

Patent Assignee: SILICON LAB INC (SILI-N)
Inventor: **HEIN J P** ; SCOTT J W; **SOOCH N S** ; WELLAND D R
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6198816	B1	20010306	US 97837702	A	19970422	200147	B
			US 97837714	A	19970422		
			US 97841409	A	19970422		
			US 9834428	A	19980304		

Priority Applications (No Type Date): US 9834428 A 19980304; US 97837702 A 19970422; US 97837714 A 19970422; US 97841409 A 19970422
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6198816	B1		38	H04M-001/738	CIP of application US 97837702 CIP of application US 97837714 CIP of application US 97841409 CIP of patent US 5870046

Abstract (Basic): US 6198816 B1

NOVELTY - A capacitive interface (1703) couples a hookswitch, caller ID and ringer interface circuit (1704) to phone lines. The hookswitch, caller ID and ringer interface circuit is formed within an integrated portion of a phone line side circuit (118). A signal transmitted across a capacitive isolation barrier is used to provide power to a portion of the phone line side circuit.

DETAILED DESCRIPTION - The capacitive isolation barrier is used to couple the user powered circuit (116) to the phone line side circuit. INDEPENDENT CLAIMS are also included for the following:

(a) a method of providing a communication system that may be coupled to a phone line;

(b) a phone line connection circuit;

(c) and a method of coupling an electrical circuit to a phone line.

USE - Used in telephony, medical electronics and industrial process control applications.

ADVANTAGE - Provides a reliable, accurate and low cost system for effecting bidirectional communication of both analog signal information and control information across a high voltage isolation barrier.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the communication system.

Phone line side circuit (118)
Capacitive interface (1703)
Hookswitch, caller ID and ringer interface circuit (1704)
pp; 38 DwgNo 17/21

Title Terms: COMMUNICATE; SYSTEM; TELEPHONE; CAPACITANCE; INTERFACE; COUPLE ; CALL; ID; RING; INTERFACE; CIRCUIT; TELEPHONE; LINE
Derwent Class: S01; S05; W01
International Patent Class (Main): H04M-001/738
International Patent Class (Additional): H04M-019/00
File Segment: EPI

3/5/6 (Item 6 from file: 350)

DIALOG(R)File 350:Derwent WPIX

013595954 **Image available**
WPI Acc No: 2001-080161/200109
XRPX Acc No: N01-061102

Subscriber loop interface circuit apparatus for central telephone exchange, includes signal processor which computes common mode and differential mode components of subscriber loop

Patent Assignee: SILICON LAB INC (SILI-N)
Inventor: **HEIN J P ; SOOCH N S**
Number of Countries: 093 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200065808	A1	20001102	WO 2000US10764	A	20000421	200109	B
AU 200044796	A	20001110	AU 200044796	A	20000421	200109	
EP 1173966	A1	20020123	EP 2000926233	A	20000421	200214	
			WO 2000US10764	A	20000421		
JP 2002543680	W	20021217	JP 2000614638	A	20000421	200312	
			WO 2000US10764	A	20000421		

Priority Applications (No Type Date): US 2000502282 A 20000210; US 99298008 A 19990422
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200065808	A1	E	27	H04M-003/00	
Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW				
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ TZ UG ZW					
AU 200044796	A			H04M-003/00	Based on patent WO 200065808
EP 1173966	A1	E		H04M-003/00	Based on patent WO 200065808
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI					
JP 2002543680	W		31	H04Q-003/42	Based on patent WO 200065808

Abstract (Basic): WO 200065808 A1

NOVELTY - The linefeed driver inputs the sensed tip and ring signals (222) of subscriber loop to a signal processor (210). The signal processor computes common mode and differential mode components of subscriber loop and outputs a loop control signal. The linefeed driver drives the subscriber loop based on the subscriber loop control signal output by the signal processor.

USE - For central telephone exchange and for zero loop applications such as in ISDN network, community antenna television (CATV) network and wireless applications.

ADVANTAGE - The signal processor computes common mode and differential mode components of subscriber loop instead of linefeed driver regardless of packaging implementation, which enables signal processor to handle majority of BORSCHT functions such as supervision of ring trip, off-hook detection.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of subscriber loop interface circuit including signal processor and linefeed driver.

Signal processor (210)
Ring signal (222)
pp; 27 DwgNo 2/6

Title Terms: SUBSCRIBER; LOOP; INTERFACE; CIRCUIT; APPARATUS; CENTRAL; TELEPHONE; EXCHANGE; SIGNAL; PROCESSOR; COMPUTATION; COMMON; MODE; DIFFERENTIAL; MODE; COMPONENT; SUBSCRIBER; LOOP
Derwent Class: W01
International Patent Class (Main): H04M-003/00; H04Q-003/42
International Patent Class (Additional): H04L-025/02; H04M-003/22; H04M-019/00
File Segment: EPI

3/5/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013499788 **Image available**
WPI Acc No: 2000-671729/200065
Related WPI Acc No: 1998-584026; 2000-116869; 2000-686101; 2001-015037; 2001-181441; 2001-190654; 2001-234102; 2001-281144; 2001-431571; 2001-440036; 2002-009481; 2002-082016; 2002-120969; 2002-235397; 2002-236851; 2002-303142; 2002-749276; 2003-027952; 2003-089291
XRPX Acc No: N00-497907

Data communication system e.g. for telephone, industrial process control application, has phone line side integrated ringer circuit in phone line side circuit, draws no loop current from phone line during ringing

Patent Assignee: SILICON LAB INC (SILI-N)
Inventor: **HEIN J P** ; KRONE A W; SCOTT J W; **SOOCH N S** ; WELLAND D R
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6104794	A	20000815	US 97837702	A	19970422	200065	B
			US 97837714	A	19970422		
			US 97841409	A	19970422		
			US 9834460	A	19980304		

Priority Applications (No Type Date): US 9834460 A 19980304; US 97837702 A 19970422; US 97837714 A 19970422; US 97841409 A 19970422
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6104794	A		39	H04M-001/00	CIP of application US 97837702
					CIP of application US 97837714
					CIP of application US 97841409

Abstract (Basic): US 6104794 A

NOVELTY - A powered side circuitry (116) is coupled to a phone line side circuit (118) through an isolation barrier which consists of one or more capacitors. The phone line side circuit is coupled to phone lines. A phone line side integrated ringer circuit within phone line side circuit, draws no loop current from phone line during ringing conditions.

DETAILED DESCRIPTION - The phone line side circuit and powered side circuit are configured to communicate across isolation barrier through digital signals. The phone line side integrated ringer circuitry operates from power supplied from across the isolation barrier. An INDEPENDENT CLAIM is also included for communication method.

USE - For telephone, communication of data in medical electronics, industrial process control applications, etc.

ADVANTAGE - The isolation barrier which is a capacitive isolation barrier, allows bidirectional communication and extraction of power from signals transmitted across the barrier, efficiently.

DESCRIPTION OF DRAWING(S) - The figure shows the communication system.

Powered side circuitry (116)
Circuit (118)
pp; 39 DwgNo 17/21

Title Terms: DATA; COMMUNICATE; SYSTEM; TELEPHONE; INDUSTRIAL; PROCESS; CONTROL; APPLY; TELEPHONE; LINE; SIDE; INTEGRATE; RING; CIRCUIT; TELEPHONE; LINE; SIDE; CIRCUIT; DRAW; NO; LOOP; CURRENT; TELEPHONE; LINE; RING
Derwent Class: W01
International Patent Class (Main): H04M-001/00
International Patent Class (Additional): H04M-001/56; H04M-009/00; H04M-009/08; H04M-015/06
File Segment: EPI

3/5/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012945016 **Image available**
WPI Acc No: 2000-116869/200010
Related WPI Acc No: 1998-584026; 2000-671729; 2000-686101; 2001-015037; 2001-181441; 2001-190654; 2001-234102; 2001-281144; 2001-431571; 2001-440036; 2002-009481; 2002-082016; 2002-120969; 2002-235397; 2002-236851; 2002-303142; 2002-749276; 2003-027952
XRPX Acc No: N00-088485

Digital access arrangement circuit for telephone connection termination system

Patent Assignee: SILICON LAB INC (SILI-N)
Inventor: DUPUIS T J; SCOTT J W; **SOOCH N S** ; TUTTLE G T; WELLAND D R; KRONE A W; **HEIN J P** ; FLUKE B J
Number of Countries: 072 Number of Patents: 011
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9966704	A1	19991223	WO 99US11377	A	19990521	200010	B
AU 9940953	A	20000105	AU 9940953	A	19990521	200024	
EP 1088440	A1	20010404	EP 99924456	A	19990521	200120	
			WO 99US11377	A	19990521		
US 6201865	B1	20010313	US 97837702	A	19970422	200120	
			US 97837714	A	19970422		
			US 97841409	A	19970422		
			US 9834455	A	19980304		
			US 9834456	A	19980304		
			US 9834620	A	19980304		
			US 9834682	A	19980304		
			US 9834683	A	19980304		
			US 9834687	A	19980304		
			US 9835175	A	19980304		
			US 9835779	A	19980304		
			US 9897621	A	19980616		
KR 2001052867	A	20010625	KR 2000714204	A	20001214	200173	
US 6359983	B1	20020319	US 97837702	A	19970422	200224	N
			US 97837714	A	19970422		
			US 97841409	A	19970422		
			US 9834687	A	19980304		
US 6389134	B1	20020514	US 97837702	A	19970422	200239	N
			US 97837714	A	19970422		
			US 97841409	A	19970422		
			US 9835779	A	19980304		
JP 2002518944	W	20020625	WO 99US11377	A	19990521	200243	
			JP 2000555418	A	19990521		
US 6408034	B1	20020618	US 97837702	A	19970422	200244	N
			US 97837714	A	19970422		
			US 97841409	A	19970422		
			US 9834682	A	19980304		
US 6480602	B1	20021112	US 97837702	A	19970422	200278	N
			US 97837714	A	19970422		
			US 97841409	A	19970422		
			US 9834455	A	19980304		
US 6498825	B1	20021224	US 97837702	A	19970422	200303	
			US 97837714	A	19970422		
			US 97841409	A	19970422		
			US 9834455	A	19980304		
			US 9834456	A	19980304		
			US 9834620	A	19980304		
			US 9834682	A	19980304		
			US 9834683	A	19980304		
			US 9834687	A	19980304		
			US 9835175	A	19980304		
			US 9835779	A	19980304		
			US 9898489	A	19980616		

Priority Applications (No Type Date): US 9898489 A 19980616; US 9897621 A 19980616; US 97837702 A 19970422; US 97837714 A 19970422; US 97841409 A 19970422; US 9834455 A 19980304; US 9834456 A 19980304; US 9834620 A 19980304; US 9834682 A 19980304; US 9834683 A 19980304; US 9834687 A 19980304; US 9835175 A 19980304; US 9835779 A 19980304

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9966704	A1	E	48	H04M-011/00	
	Designated States (National): AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE HU IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK TJ TM TR TT UA UG UZ VN				
	Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE				
AU 9940953	A			H04M-011/00	Based on patent WO 9966704
EP 1088440	A1	E		H04M-011/00	Based on patent WO 9966704
	Designated States (Regional): DE DK ES FI FR GB IT SE				
US 6201865	B1			H04M-011/00	CIP of application US 97837702 CIP of application US 97837714 CIP of application US 97841409 CIP of application US 9834455 CIP of application US 9834456 CIP of application US 9834620 CIP of application US 9834682 CIP of application US 9834683 CIP of application US 9834687 CIP of application US 9835175 CIP of application US 9835779 CIP of patent US 5870046
KR 2001052867	A			H04M-011/00	
US 6359983	B1			H04M-001/00	CIP of application US 97837702 CIP of application US 97837714 CIP of application US 97841409 CIP of patent US 5870046 CIP of patent US 6137827
US 6389134	B1			H04M-001/00	CIP of application US 97837702 CIP of application US 97837714 CIP of application US 97841409 CIP of patent US 5870046
JP 2002518944	W		56	H04M-011/00	Based on patent WO 9966704
US 6408034	B1			H04L-007/06	CIP of application US 97837702 CIP of application US 97837714 CIP of application US 97841409 CIP of patent US 5870046
US 6480602	B1			H04M-001/00	CIP of application US 97837702 CIP of application US 97837714 CIP of application US 97841409
US 6498825	B1			H04B-015/00	CIP of application US 97837702 CIP of application US 97837714 CIP of application US 97841409 CIP of application US 9834455 CIP of application US 9834456 CIP of application US 9834620 CIP of application US 9834682 CIP of application US 9834683 CIP of application US 9834687 CIP of application US 9835175 CIP of application US 9835779 CIP of patent US 5870046 CIP of patent US 6137827 CIP of patent US 6144326 CIP of patent US 6160885 CIP of patent US 6167134 CIP of patent US 6359983 CIP of patent US 6385235

CIP of patent US 6389134
CIP of patent US 6408034
CIP of patent US 6430229

Abstract (Basic): WO 9966704 A1

NOVELTY - A DC holding circuit with a current limiting function is provided within a phone line side circuit (118). The DC holding circuit is programmed with respect to a digital data transmitted across a capacitive isolation barrier (120) so that DC holding circuit is operated in a current limiting mode and in a non-current limiting mode to satisfy different phone line interface standards.

DETAILED DESCRIPTION - The DC holding circuit has an external device to dissipate more power in a current limiting mode than in a non-current limiting mode. The DAA circuit has a power side circuit (116) coupled to a phone line side circuit, connected to a telephone line, through a capacitive isolation barrier. The isolation barrier transmits a digital signals between the isolation interfaces (1614,1610) in the phone line side and power side circuit. INDEPENDENT CLAIMs are also included for the following:

(a) communication system and telephone line coupling method;

(b) DC holding circuit construction method

USE - For connection termination system for telephones of different standards.

ADVANTAGE - Facilitates operation with multiple telephone interface standards provides a noise immuned isolation system to reproduce output signals accurately. Reduces power dissipation requirements of integrated circuit in a communication system.

DESCRIPTION OF DRAWING(S) - The figure shows a block diagram of DAA circuit.

Power side circuit (116)
Phone line side circuit (118)
Isolation barrier (120)
Isolation interfaces (1610,1614)
pp; 48 DwgNo 2/8

Title Terms: DIGITAL; ACCESS; ARRANGE; CIRCUIT; TELEPHONE; CONNECT; TERMINATE; SYSTEM
Derwent Class: W01
International Patent Class (Main): H04B-015/00; H04L-007/06; H04M-001/00; H04M-011/00
International Patent Class (Additional): H04B-001/38; H04B-003/00; H04M-003/00; H04M-009/00; H04M-019/00
File Segment: EPI

3/5/9 (Item 9 from file: 350)

DIALOG(R)File 350:Derwent WPIX

009213128 **Image available**
WPI Acc No: 1992-340550/199241
Related WPI Acc No: 1989-068680; 1990-231396
XRPX Acc No: N92-259735

Clock multiplier and jitter attenuator - has internal clock signal formed by frequency dividing stable clock to control writing and reading data of FIFO storage cells

Patent Assignee: CRYSTAL SEMICONDUCTOR CORP (CRYS-N)
Inventor: **HEIN J P** ; **SOOCH N S** ; STERN K J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5150386	A	19920922	US 8751985	A	19870519	199241	B
			US 89308326	A	19890209		

Priority Applications (No Type Date): US 8751985 A 19870519; US 89308326 A 19890209

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5150386	A		14	H04L-007/00	Cont of application US 8751985 Cont of patent US 4805198

Abstract (Basic): US 5150386 A

The clock mutliplier and jetter attenuator circuit provides a stable clock which is a multiple frequency of the average frequency of an external digital data stream. The external data is written into successive storage cells of a FIFO at its own clock rate and read out of the FIFO at the rate of an internal clock signal which is formed by frequency dividing the stable clock.

The relative locations of the cell being written into and the cell being read out of are determined at periodic time intervals. These relative locations are used to adjust the frequency of an internal oscillator which generates the stable clock. The instantaneous jitter on the digital data stream is absorbed by the FIFO.

USE/ADVANTAGE - For interface circuits of telephone transmission lines. Single IC chip.

Dwg.1/3

Title Terms: CLOCK; MULTIPLIER; JITTER; ATTENUATE; INTERNAL; CLOCK; SIGNAL; FORMING; FREQUENCY; DIVIDE; STABILISED; CLOCK; CONTROL; WRITING; READ; DATA; FIFO; STORAGE; CELL

Derwent Class: U22; W01

International Patent Class (Main): H04L-007/00

File Segment: EPI

3/5/10 (Item 10 from file: 350)

007803568 **Image available**

WPI Acc No: 1989-068680/198909

Related WPI Acc No: 1990-231396; 1992-340550

XRPX Acc No: N89-052370

Clock multiplier-jitter attenuator for telephone transmission line - has N-bit storage register, data read and write facility, oscillator and address sampler

Patent Assignee: CRYSTAL SEMICONDUCT (CRYS-N)

Inventor: **HEIN J P** ; **SOOCH N S** ; STERN K J

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 4805198	A	19890214	US 8751985	A	19870519	198909	B

Priority Applications (No Type Date): US 8751985 A 19870519

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 4805198	A		14		

Abstract (Basic): US 4805198 A

The clock multiplier/jitter attenuator circuit provides a stable clock which is a multiple frequency of the average frequency of an external digital data stream. The external data is written into successive storage cells of a FIFO at its own clock rate and read out of the FIFO at the rate of an internal clock signal which is formed by frequency dividing the stable clock.

The relative locations of the cell being written into and the cell being read out of are determined at periodic time intervals, and these relative locations are used to adjust the frequency of an internal oscillator which generates the stable clock. The instantaneous jitter on the digital data stream is absorbed by the FIFO.

ADVANTAGE - Can be fabricated entirely on single integrated circuit chip.

Title Terms: CLOCK; MULTIPLIER; JITTER; ATTENUATE; TELEPHONE; TRANSMISSION; LINE; N; BIT; STORAGE; REGISTER; DATA; READ; WRITING; FACILITY; OSCILLATOR; ADDRESS; SAMPLE
Derwent Class: U22; W01
International Patent Class (Additional): H04L-007/00
File Segment: EPI

3/5/11 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004672959
WPI Acc No: 1986-176301/198627
XRPX Acc No: N86-131682
Temp. insensitive CMOS precision current source - forces both voltage and on-chip resistance to have same temp. dependency which when divided give value of output constant current
Patent Assignee: AT & T BELL LAB (AMTT)
Inventor: **HEIN J P ; SOOCH N S**
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 4595874	A	19860617	US 84654411	A	19840926	198627	B
JP 61086822	A	19860502				198627	

Priority Applications (No Type Date): US 84654411 A 19840926
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 4595874	A		7		

Abstract (Basic): US 4595874 A
The CMOS circuit (10) has both a temperature dependent voltage (V(T) and on-chip resistance (R(T) where the dependencies of both voltage and resistance are linear functions of temperature of the form y=mx+b. The ratio
of the slopes (mv/mR) is constructed to be equal to the ratio of the y-intercepts (bv/bR), where this ratio is a constant value, denoted s. Therefore, since a constant output current Io is equal to V(T)/R(T), Io will be equal to the constant value s.
Additionally, a constant reference voltage (Vo) may also be provided with a minimal increase in the circuitry needed to provide the constant current. A voltage generator comprises a voltage source (12) a bipolar junction transistor (18) and or resistor divider network including two resistors (14,16) connected between emitter and ground.
ADVANTAGE - High quality voltage reference. Self-contained, requiring no external voltage or current sources. Source varies only with sheet resistance and insensitive to other process parameters.
Title Terms: TEMPERATURE; INSENSITIVE; CMOS; PRECISION; CURRENT; SOURCE; FORCE; VOLTAGE; CHIP; RESISTANCE; TEMPERATURE; DEPEND; DIVIDE; VALUE; OUTPUT; CONSTANT; CURRENT
Derwent Class: U13; U24
International Patent Class (Additional): G05F-001/56; G05F-003/16; H03F-001/30
File Segment: EPI